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An integrated multi-scale structured heat sink for the efficient heat dissipation of two-phase immersion-cooled chips☆

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ABSTRACT

Two-phase immersion cooling (TPIC) is positioned to become a critical thermal management solution for next-generation high-power chips. However, maintaining temperature uniformity remains challenging, with case temperatures often exceeding 70 °C under high power loads. This study introduces an integrated multi-scale structured heat sink, incorporating a vapor chamber (VC) as a heat spreader, to replace conventional cooling solutions. Experimental results demonstrate that this hybrid design achieves superior thermal performance: at a power input of 600 W, the maximum case temperature remains stable below 65 °C, with system thermal resistance below 0.026 °C/W. High-speed visualization reveals enhanced boiling dynamics achieved through multiscale surface engineering. Micro/nano-structured coatings promote bubble nucleation, while macro-scale pin–fin arrays augment the heat transfer area. This synergistic design significantly improves temperature uniformity, reducing the maximum temperature difference across the chip by 75 % (from 14.3 °C to 3.8 °C). Compared to baseline, the proposed architecture lowers the mean temperature by 22.1 %, and reduces the average thermal resistance by 6.4 %. This work presents a viable strategy for efficient thermal management of kilowatt-class chips, supporting the advancement of next-generation high-power computing systems.

1. Introduction

Innovative thermal management strategies enable substantial cooling energy consumption in high-density electronic systems [1]. Among these, two-phase immersion cooling (TPIC) represents a transformative paradigm for data center thermal management. Unlike forced-convection microchannel cooling [2] and single-phase immersion systems [3,4], which rely on complex flow architectures and are highly sensitive to coolant conditions [5], TPIC operates via passive pool boiling and remains largely unaffected by external fluctuations. Moreover, it exhibits strong potential for improving sustainability outcomes [6]. This method immerses server hardware directly in a dielectric fluid with tailored boiling properties [7], leveraging latent heat absorption during phase change and uniform temperature distribution through direct dielectric contact [8]. The self-sustaining thermal cycle involves nucleate boiling at the chip surface, vapor transport to condensers, and gravity-driven liquid return [9], typically operating atmospheric pressure [10]. Chip-scale nucleate boiling is particularly critical, as the density and distribution of nucleation sites govern both the heat transfer efficiency and thermal uniformity [11].

In practical implementations, however, bare or packaged chips often exhibit suboptimal boiling performance when directly immersed. Enhanced surface architectures are therefore essential, especially for high-power components [12]. Current enhancement approaches span multiple scales and involve competing physical mechanisms [13], including surface area expansion, fin efficiency [14], micro-nano structures (nucleation sites) [15,16], liquid spreading [17] and re-wetting ability [18], and bubble escape dynamics [19]. At the macro-scale, fin arrays [20] and porous foams [21] enhance boiling by increasing surface area and nucleation site density. Micro/nano-scale modifications, such as brazed copper particle (49–283 μm) [22] or carbon nanotube networks [23] boost critical heat flux and reduce wall superheat via microcavities and nano-porous vapor pathways. Recently, multi-scale structures combining two or more fabrication techniques have gained attention [24], effectively balancing capillary and viscous forces during phase change [25] and enhancing heat transfer through promoting transient conduction, micro-convection, microlayer

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Nomenclature

Symbol	Description (Unit)
T	Temperature (°C)
η	Rate of decrease (%)
ΔT	Temperature difference (°C)
Q	Power input (W)
R	Thermal resistance (°C/W)
D_c	Diameter of cylinder pin–fin (mm)
H_c	Height of cylinder pin–fin (mm)
l_g	Length of square gear (mm)
$s_{g,v}$	Vertical space of gears (mm)
$s_{g,h}$	Horizontal space of gears (mm)
CA	Contact angle (°)
D_{li}	Diameter of liquid (mm)
V_0	Initial velocity (m/s)
I	Current (A)
U	Voltage (V)
q	Heat flux (W/cm^2)
g	Gravity (m/s^2)

Subscripts

sat	Saturated
max	Maximum
mean	Mean
avg	Average
Die	Die
TIM	Thermal interface material
sp	Spreading
f	Fin
b	Boiling

Abbreviation

HS	Baseline copper heat sink
EHS	Enhanced heat sink
VC	Vapor chamber
TTV	Thermal test vehicle
TPIC	Two-phase immersion cooling

evaporation, contact line evaporation, and macro-convection [26].

Industrial progress in two-phase immersion cooling has closely paralleled recent academic advances. For example, Intel Microelectronics integrated an enhanced heat sink into a lidded package [27], achieving a 25–50 % reduction in thermal resistance for chips operating at up to 600 W under TPIC. Nevertheless, cooling performance continues to be limited by manufacturing constraints and available heat transfer area [28], which directly affect lid temperature and thermal resistance—key factors in future heat sink design. Another major challenge lies in immersion coolants, which must exhibit suitable thermophysical and dielectric properties, along with chemical stability. According to a comprehensive evaluation by the Chemours [29], many commercial coolants suffer from high global warming potential (GWP), inadequate dielectric characteristics, high boiling points, environmental persistence, and elevated cost. Although a well-selected coolant can maintain chip case temperatures below 70 °C at 600 W [30], considerable significant thermal gradients may persist, especially on vertically mounted boards [31].

Beyond thermal performance, wider adoption of TPIC requires careful evaluation of life-cycle costs and integration compatibility. As emphasized in a recent study [6], life cycle assessment (LCA) reveals that two-phase immersion systems can exhibit lower environmental impact and operational cost than single-phase immersion and microchannel cooling, owing to reduced coolant consumption and lower pumping energy. However, successful integration of enhanced heat sinks into existing server architectures over the system lifetime requires more deliberate design to avoid compromising cooling efficiency or long-term reliability. While vapor chambers (VCs) have shown potential in immersion cooling applications [32], a systematic experimental study on a heat sink integrally designed with a VC to simultaneously suppress peak temperature and spatial thermal non-uniformity remains lacking.

This study aims to address this gap by introducing an integrated two-phase immersion cooling solution. A monolithic cylindrical pin–fin sink was fabricated to minimize interfacial thermal resistance. The macroscopic pin-fins were machined with micro-scale serrations, followed by the application of a nano-scale graphene coating via high-temperature spray deposition. This multi-tier structure extends the heat transfer area, promotes nucleation, and enhances liquid spreading. Using a novel low-cost fluorinated coolant, experimental results demonstrate the ability to maintain chip surface temperatures below 65 °C. High-speed imaging captured bubble dynamics and departure patterns, clarifying the relationship between input power, bubble density, and temperature distribution. Furthermore, integration of a vapor chamber as a heat spreader reduced both peak temperatures and spatial thermal gradients, enabling effective cooling of a 600 W chip.

2. Experimental setup

A schematic of the custom-designed TPIC system for server chip thermal management is shown in Fig. 1 (a). The primary components consist of a sealed metal containment tank (150 mm × 250 mm × 400 mm) with an integrated copper plate condenser, a constant-temperature chiller, a high-speed imaging system, and data acquisition modules. The containment tank was constructed with an aluminum alloy upper section and acrylic lower observation windows, sealed with O-ring gaskets and socket-head fasteners to ensure pressure integrity. Aviation plug interfaces on the right panel enable secure power delivery to the thermal test unit while maintaining dielectric isolation. Fig. 1 (b) demonstrates the server-scale simulation configuration featuring a vertically mounted PCB assembly with pressurized thermal test unit. An Intel Thermal Test Vehicle (TTV) replicates actual CPU thermal profiles through five distributed die heaters. The central die 3 configuration emphasizes the maximum high-power design emulation (up to 340 W design target, chip package up to 600 W). According to the design dimensions of the heating zone (defined as die 1 to die 5) provided by the supplier (die 2 to die 4: 31 mm × 20.66 mm edge dimensions, die 1 and die 5: 31 mm × 8.24 mm edge dimensions; 104.5 mm × 70.5 mm TTV package size), the calculated area of the total heat region is 24.27 square centimeters. Three T-type thermocouples (accuracy ±0.5°C) were installed in machined grooves on the lid and connected to a KEYSIGHT 34972A data acquisition system. Given that the system's maximum error is significantly lower than that of the thermocouples, its contribution to measurement uncertainty was considered negligible. This setup enabled accurate monitoring of the case temperature (T). Flexible bus bars ensure low-impedance power delivery to the die heaters.

The cooling enhancement strategy employs two complementary surface engineering approaches: (1) Submillimeter copper pin–fin arrays for intensified convective area, (2) Multiscale spray-coating for controlled nucleation. These hierarchical structures are mechanically bonded to the TTV using high-performance thermal interface material. The selection of coolants for TPIC systems prioritizes thermophysical parameters as the primary criteria. Additionally, procurement cost constitutes another critical consideration. This is attributable to the fact that, even when a well-sealed tank is utilized, the coolant is prone to

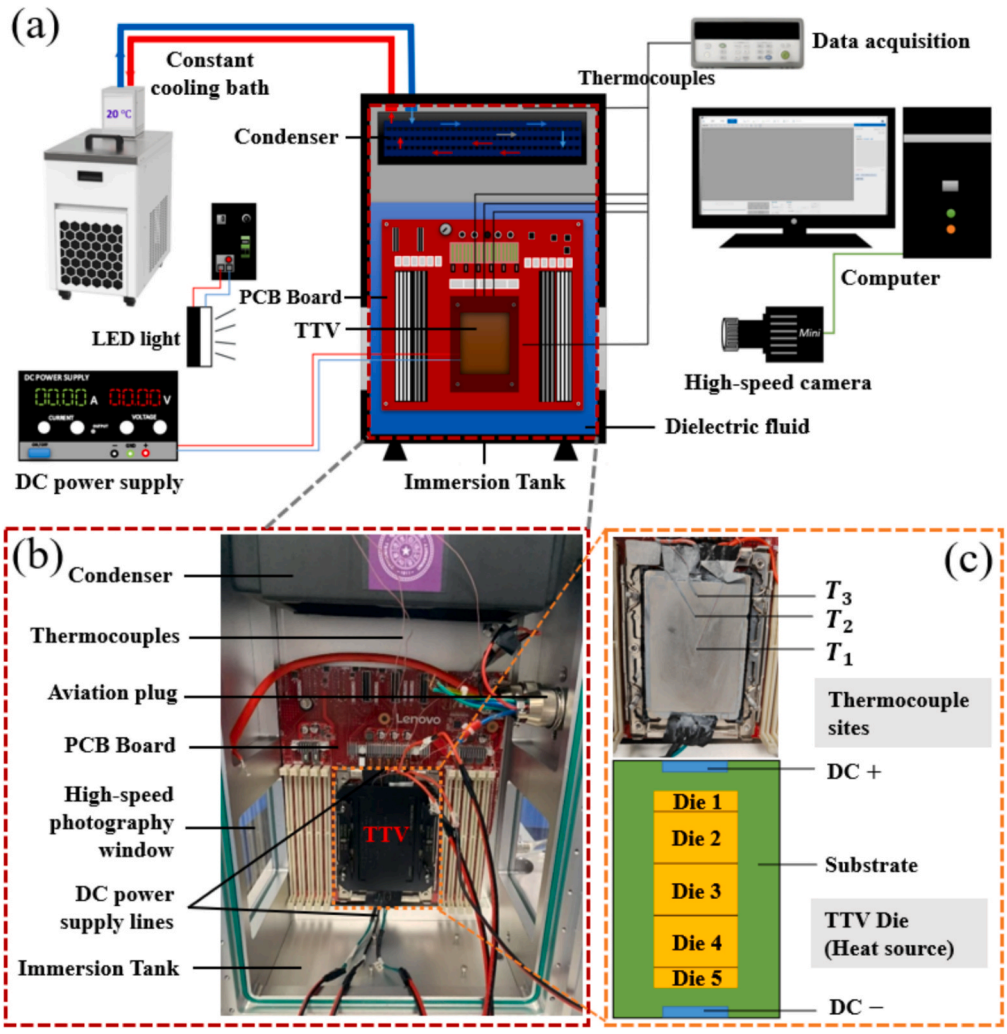

Fig. 1. Two-phase immersion cooling experimental setup. (a) Schematic illustration of the experimental setup, (b) photograph depicting the interior of the immersion tank, (c) the thermocouple sites of the TTV packaged lid and the distribution of dies within TTV.

volatilize into the surrounding environment during the operational process. As previously reported [30], commercially available dielectric coolants on the market generally demonstrate comparable thermophysical properties and exhibit similar boiling characteristics under identical working conditions. In this study, the system employs the Noah-2100A fluorinated coolant [33]. This coolant was chosen for its optimal phase-change characteristics (atmospheric saturation point at 47 °C) and favorable thermophysical properties, which are elaborated in Table 1. Significantly, the cost of Noah-2100A is substantially lower compared to other coolants such as HFE-7100 (manufactured by 3 M Co., USA) [34], which was procured through Chinese market channels.

Table 1
Physical properties of Noah-2100A at atmospheric pressure [33].

Thermophysical parameters	Noah – 2100A
Molecular weight (g/mol)	300
Saturation temperature (°C)	47
Liquid density (kg/m^3)	1601
Liquid thermal conductivity (W/m • K)	0.0609
Liquid heat capacity (kJ/kg • K)	1.279
Liquid surface tension (mN/m)	11.44
Latent heat of vaporization (kJ/kg)	93.22
Dielectric constant (12 GHz)	1.88
GWP	20
ODP	0

Once a coolant has been chosen, the reduction of the total thermal resistance primarily focuses on the design of the heat sink geometry and the selection of materials with high thermal conductivity [35].

3. Heat sink design and surface treatment

3.1. Heat sink design

The liquid-cooled heat sink was designed via 3D modeling to serve as a direct replacement for conventional air-cooled designs, maintaining identical base dimensions (Fig. 2 (a)). Fabricated from a solid copper block through computer numerical control (CNC) machining (Fig. 2 (b)), the structure integrates a 4-mm base with cylindrical pin fins. Each pin fin has a diameter $D_c = 8$ mm and a heigh $H_c = 6.5$ mm, and is patterned with crosswise square gears of length$l_g = 500$-μm. The inter-fin channels are spaced at $s_{g,h} = 1$mm (Fig. 2 (c)). This monolithic construction minimizes interfacial thermal resistance compared to additive manufacturing or welded assemblies. The engineered surface architecture (Fig. 2 (d)) simultaneously enhances the available boiling heat transfer area (8 % increase versus bare cylindrical pin-fins baseline), constrains bubble coalescence, and facilitates vapor evacuation. As shown in Fig. 2 (e), the copper heat sink (HS) is subsequently mounted vertically on the PCB board to be tested as a baseline. Meanwhile, the original air-cooled heat sink (Fig. 2 (f)) is removed from the server, shown here to illustrate the baseline system prior to modification. To

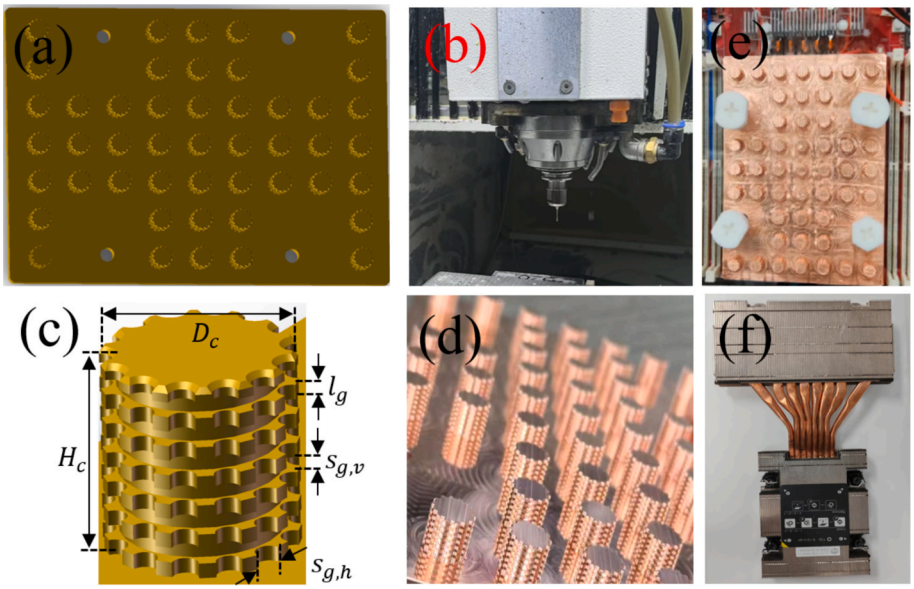

Fig. 2. The design and fabrication of two-phase immersion heat sinks. (a) design drawing for the heat sink, (b) CNC machine tools utilized for mechanical processing equipment, (c) the diagram depicting the structural dimensions of a cylinder pin–fin and gears, (d) physical photographs of the heat sink along with local enlarged perspectives, (e) the baseline copper heat sink (HS) is vertically mounted on the PCB board, (f) the original heat sink was removed from the server.

lower the incipient boiling point, it is necessary to fabricate bubble nucleation sites on the surface. This can be accomplished via techniques such as sandblasting [36], pulse laser treatment [37], welding [19], and spraying coating [38]. A recent study demonstrated that fabricating patterned graphene surfaces can increase nucleation sites, enhancing boiling heat transfer by up to 135 % [39]. This research inspired us to explore a simple and efficient approach for surface modification via spraying coating.

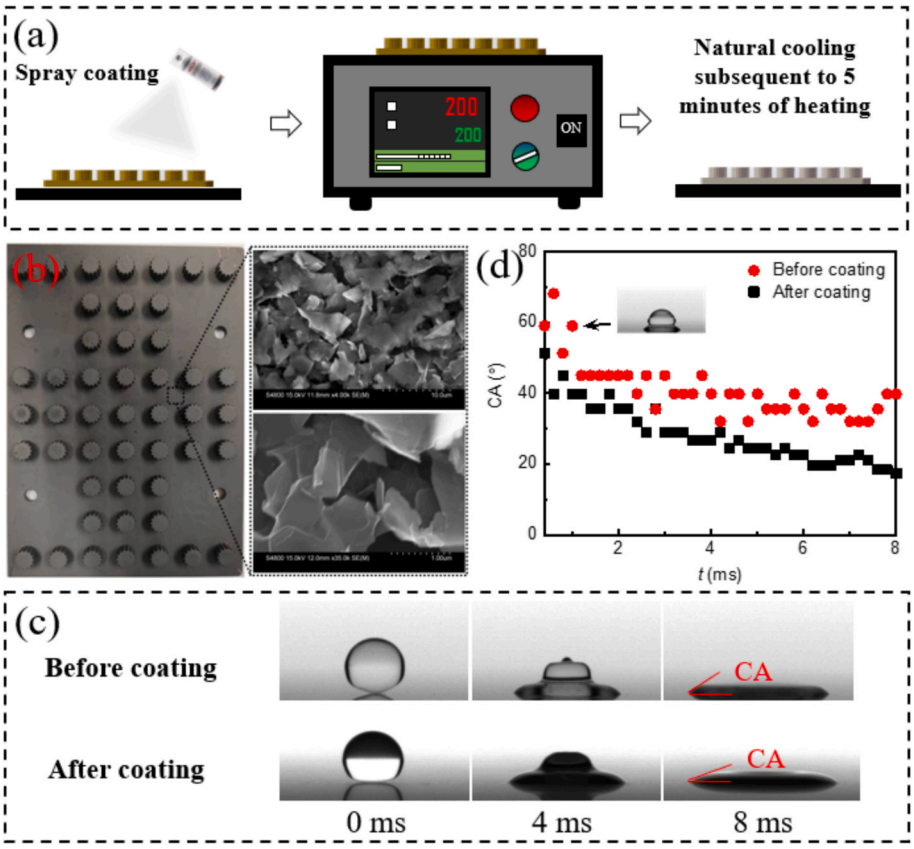

Fig. 3. Preparation and characterization of boiling-enhanced micro-nano structures. (a) Spray coating process for preparation of boiling-enhanced surface, (b) the heat sink after coating and SEM scanning for the analysis of micro-nano structures, (c) the wettability ability of Noah-2100A droplets on heat sink surfaces, (d) Temporal evolution of the contact angles (CA) in correspondence with the images in (c).

3.2. Coating process

Graphene was selected as the nano-coating material. It was supplied in a pressurized canister (Fig. 3 (a)), from which the graphene nanomaterial was ejected by manually actuating a spray valve. It is provided by Suqian Nakaitai New Materials Co., Ltd. When sprayed at a height of around 20 cm above the heat sink, it can cover a specific area of the heat sink's surface. After 2–3 rounds of spraying, the entire surface can be coated. Subsequently, the sprayed heat sink is baked on a high-temperature table at 200°C for 5 min and then left to natural cooling, promoting uniform adhesion and solvent evaporation and forming a graphene nanosheet texture on the surface. This high-temperature-spraying coating approach [40] is capable of forming a uniform nanostructure on the surface. Moreover, it offers the advantages of low production cost and high production efficiency. Scanning electron microscopy (SEM) characterization reveals hierarchical micro-nanostructures (500 nm-1 μm graphene sheets) increasing nucleation site density by compared to bare copper surface (Fig. 3 (b)). These features promote an augmentation in the liquid wetting ability and the quantity of bubble nucleation sites. Consequently, it might enhance the boiling heat transfer performance.

Wetting dynamics were quantified in the droplet spreading experiment via high-speed camera photography. A Noah-2100A liquid droplet of diameter $D_{li} \approx 1.4$mm was released from a blunt needle with a low initial velocity ($V_0 \approx 0.15$m/s), eventually spreads on the target bare copper and coated surfaces (as shown in Fig. 3 (c)). Note that during the spreading experiments, there might be a slight variation in the initial velocities. To account for this, the experiment was replicated three times in different regions of the heat sink surface. The resulting velocity variability was within 3 %. We traced the temporal evolution of the contact angles (CA) after droplets came into contact with the surface. It indicated that the Noah-2100A liquid droplet spread rapidly within a few milliseconds due to its low surface tension. The superior wettability of liquid on micro-nano structured surfaces is evidenced in Fig. 3 (d). Specifically, the CA decreases from 45° (on the bare copper surface) to a state approaching near-perfect wetting (<15°) on the coated surfaces. When the droplet comes into contact with the structured surfaces, both capillary-driven wicking within the micro-nano structures and wetting on the surface of these structures occur simultaneously. This is because capillary force-induced wicking triggers spontaneous wetting, and wetting is a fundamental prerequisite for wicking to take place [18]. Thus, it can be reasonably inferred that the micro-nano structure formed after coating significantly enhances the wicking performance, rendering it superior to that of the bare copper surface heat sink.

4. Result and discussion

4.1. Thermal performance of enhanced heat sink

The Intel Thermal Test Vehicle (TTV) emulates real CPU thermal behavior using five distributed die heaters. Fig. 4 illustrates the non-uniform power distribution among the dies, which creates varied thermal loads, with the central die (die 3, T_1) experiencing the most rapid temperature rise due to its highest power density. The electrical power supplied to each die region was determined from the product of applied current and voltage, and the sum of all five dies defined the total TTV power. To avoid thermal damage, the total power was increased stepwise from 100 W to a maximum of 600 W. Based on the total heater area, the average heat flux density ranged from 4.1 W/cm^2 to 24.7 W/cm^2. Local heat flux, however, reached considerably higher values – for instance, up to 53.1 W/cm^2 on die 3 at 600 W total power. During testing, voltage and current were applied incrementally until the total power reached 600 W. The system was then allowed to stabilize for approximately 40 min before recording the first set of temperature data. Measurements were subsequently taken during stepwise power reductions from 600 W down to 100 W. This procedure was repeated

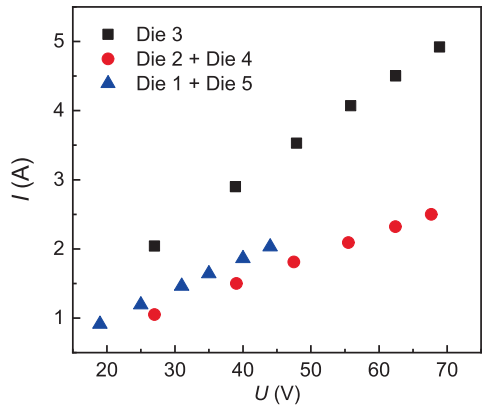

Fig. 4. Voltage and current power supply conditions of different die heat sources.

under identical power conditions at least three times to ensure reproducibility. The resulting temperature deviations are summarized in Fig. 5 (a), while other temperature-derived quantities were computed using the average of three repeated measurements.

Fig. 5 presents a comprehensive overview of the thermal performance achieved with the micro-nano structured heat sink. The engineered surface coating enhances boiling heat transfer characteristics, leading to a significant reduction in the TTV case temperature compared to the baseline copper heat sink (HS). Further analysis reveals that the enhanced heat sink (EHS) promotes heterogeneous bubble nucleation, particularly in high-heat-flux regions, which intensifies localized heat transfer while simultaneously altering the spatial temperature profile. This non-uniform activation of nucleation sites underlies the observed improvements in overall heat removal, though it also introduces distinct thermal gradient characteristics across the chip surface.

Although this spatial heating profile generates notable thermal gradients, the enhanced heat sink (EHS) successfully maintains lower temperatures across all measurement points (Fig. 5 (a)). A 600 W thermal load reveals EHS's growing advantage – achieving 4.5 % greater temperature reduction (at$\Delta T_2 = 3.1$ °C) than incurred at lower power levels. Quantitative analysis in Fig. 5 (b) – (c) shows the EHS reduces mean case temperature from 66.9 °C (HS) to 64.7 °C while lowering average thermal resistance by 12 % (0.033 vs. 0.029 °C/W). Thermal performance metrics follow:

$$T_{\text{mean}} = \frac{T_1 + T_2 + T_3}{3} \tag{1}$$

$$R_{\text{avg}} = \frac{T_{mean} - T_{sat}}{Q} \tag{2}$$

$$\Delta T_{\text{max}} = T_{\text{max}} - T_{\text{min}} \tag{3}$$

$$\Delta T = T_{\text{mean}} - T_{\text{sat}} \tag{4}$$

$$q = \frac{Q}{A} \tag{5}$$

T_{mean} represents the mean temperature measured at three thermocouple sites, namely T_1, T_2, and T_3, as depicted in Fig. 1 (c). R_{avg} is the average thermal resistance calculated based on the mean temperature. ΔT_{max} refers to the maximum temperature difference among the temperatures measured by the three thermocouples. Notably, while EHS improves bulk cooling efficiency, its localized enhancement effect amplifies maximum temperature differences from 12.7 °C (HS) to 14.3 °C at 600 W (Fig. 5 (d)), suggesting trade-offs between thermal uniformity and peak temperature mitigation.

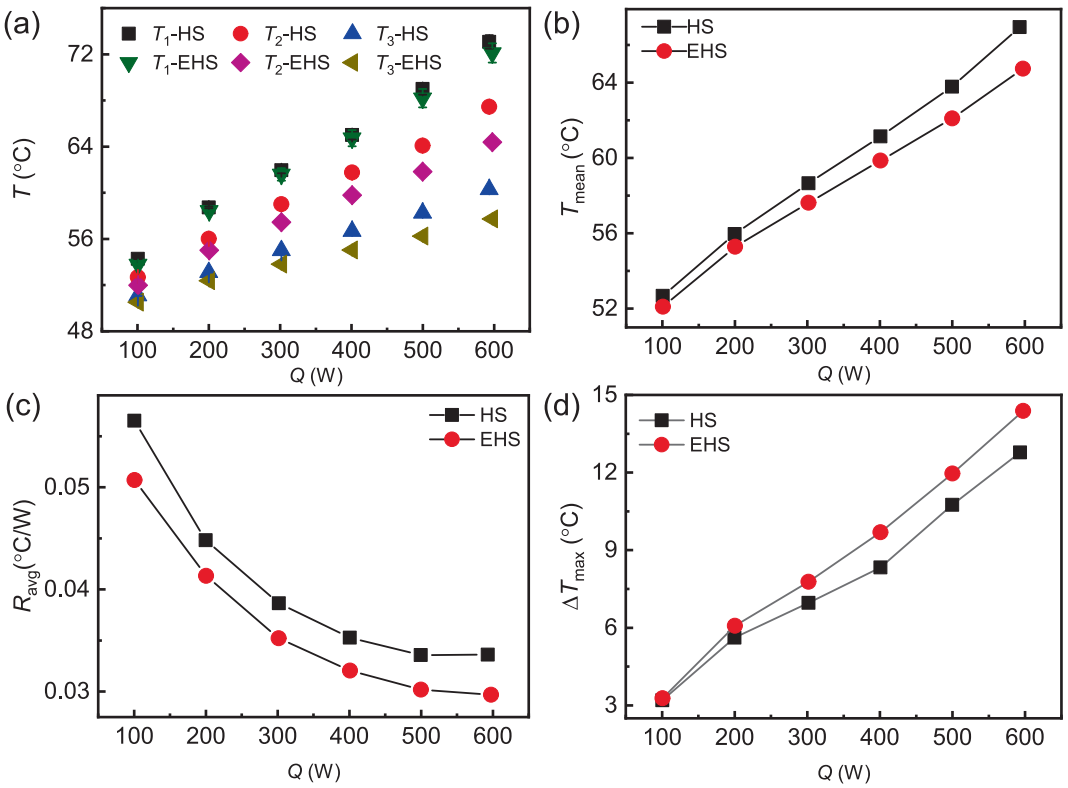

Fig. 5. Comparison of the experimental test outcomes of heat sinks before and after spray coating. (a) Temperature distribution corresponding to each thermocouple element, (b) mean temperature of heat sinks, (c) average thermal resistance of heat sinks, (d) maximum temperature difference of heat sinks.

4.2. Bubble dynamics and heat transfer mechanisms

High-speed photography techniques were employed to capture dynamic bubble behavior across heat sink surfaces under varying thermal loads. Fig. 6 (a) – (d) demonstrate power-dependent boiling patterns from 100 W to 600 W. At lower power supply ($Q \leq 200$W), sparse bubble nucleation takes place, accompanied by discrete detachment events among pin–fin structures. As depicted by the black shaded regions in Fig. 6 (a)–(b) and supplemental movie S1 and S2, the upward trajectories of bubbles within the pin–fin channels are distinctly observable. When the power input is increased to the range of 400–600 W, it instigates intensified phase change activities, as displayed in Fig. 6 (c)–(d) and supplemental movie S3 and S4. Specifically, approximately 80 % of the pin–fin channels become filled with bubbles (represented by the white shaded areas), and enhanced bubble–liquid momentum transfer is manifested through turbulent vapor columns.

High-speed imaging of an individual pin at $Q = 50$W (Fig. 6 (e)) reveals nucleation initiates preferentially within micro-grooves and

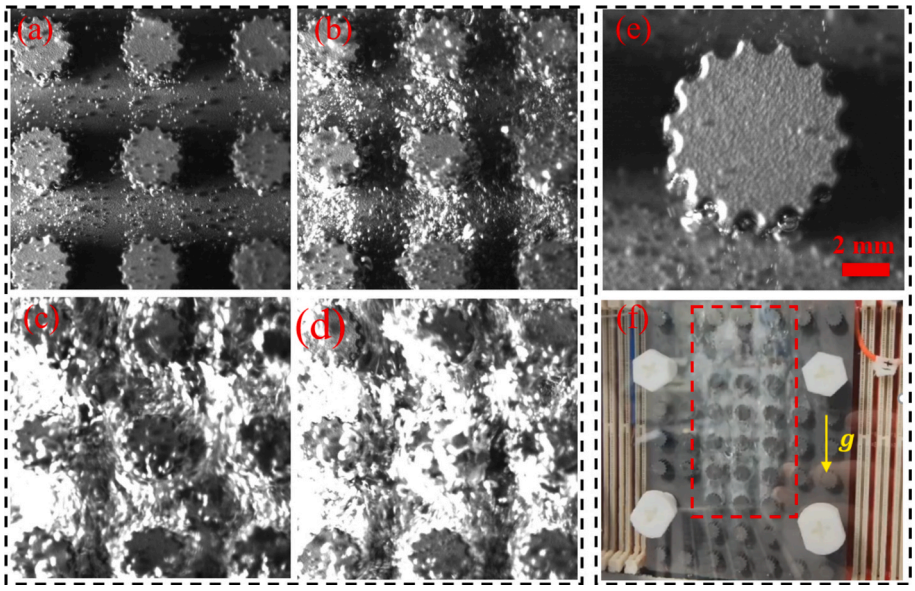

Fig. 6. Visual analysis of bubble growth and detachment on hybrid-structure surfaces. (a)$Q = 100$W, (b) $Q = 200$W, (c) $Q = 400$W, (d) $Q = 600$W, (e) An enlarged view of the bubble generation on a single cylinder at $Q = 50$W (scale bar: 2 mm), (f) A full-view photograph of EHS with a power 600 W (g: gravity).

coated substrate regions. This indicates that the micro-nano structure facilitates the nucleation of bubbles. The growing bubbles within the micro-grooves gradually expand along the channels and ultimately detach from the surface of the copper column. Subsequent vapor growth adheres to channel geometries until buoyancy-driven detachment occurs. The departure diameter is approximately 0.2 mm, which is significantly smaller than that of traditional FC-72 coolant on nano-structured surfaces as reported in reference [23]. Post-detachment coalescence creates vapor slugs (Fig. 6 (f) schematic) that accelerate through confined pin–fin gaps.

Macroscopic visualization of the EHS in Fig. 6 (f) reveals a non-uniform distribution of phase change activity, with the highest density of bubbles occurring in the central region (marked by the red dashed zone), while peripheral areas show comparatively fewer bubbles. This vertical thermal gradient corresponds to the measured temperature distribution on the Thermal Test Vehicle (TTV), where the central die T_1 reaches 72.1 °C and the edge die T_3 remains at 57.7 °C under 600 W power. This spatial thermal profile aligns with thermocouple measurements, confirming the presence of a dominant central hot spot in the vertically oriented TTV. This finding is consistent with prior study [41] which indicates that component height variance in vertically mounted two-phase immersion cooling systems significantly impacts thermal performance through bubble coalescence dynamics. Specifically, the morphological evolution of vapor bubbles during phase transition creates heterogeneous heat transfer characteristics that necessitate careful consideration in multi-chip server architectures [42]. In the present single-chip setup, localized hot spots arise mainly from non-uniform power density distribution across the chip surface, with heat dissipation efficiency fundamentally constrained by thermal spreading resistance at the TTV − heat sink interface.

To further examine temperature non-uniformity resulting from power distribution, a phase-field method adapted from prior work [43] was implemented in COMSOL Multiphysics 6.2. The study focuses on a simplified three-dimensional model of the two-phase immersion system, which represents the experimental cooling tank setup. The model includes five die heat sources, a package lid, and a heat sink, with a thin thermal resistance layer simulating the thermal interface material (thermal grease). Local mesh refinement was performed near the gas–liquid interface and the dies to improve computational accuracy and convergence, and four mesh sizes were tested: coarser (104,490 elements), coarse (300,715 elements), medium (957,085 elements), and fine (5,857,738 elements). The medium mesh (957,085 elements) was selected (see Fig. 7), as the maximum temperature difference relative to the fine mesh was below 1.2 %. The computational domain was divided into an upper vapor zone and a lower liquid region, with the initial temperature set uniformly to the coolant saturation temperature of 47 °C. The vapor zone walls were modeled as condensing surfaces held at 20 °C, other walls are subject to the boundary condition of thermal insulation. while all other walls were thermally insulated. The entire assembly, including dies and heat sink, was fully immersed in N-2100A coolant, and a transient iterative solver was employed.

Fig. 7 illustrates key aspects of the simulation, including geometry, structured meshing, initial phase-field distribution (blue: liquid, red: vapor), and the resulting temperature profile under asymmetric heating at 300 W total power (die 3: 170 W, dies 2 and 4: 85 W, dies 1 and 5: 45 W). The simulated temperature distribution confirms the experimental observation of a central hot spot, with the highest temperature localized at the center of the high-power die 3 and gradually decreasing outward. Although the model predicts a maximum lid temperature approximately 10 % lower than the experimental value (measured at T_1

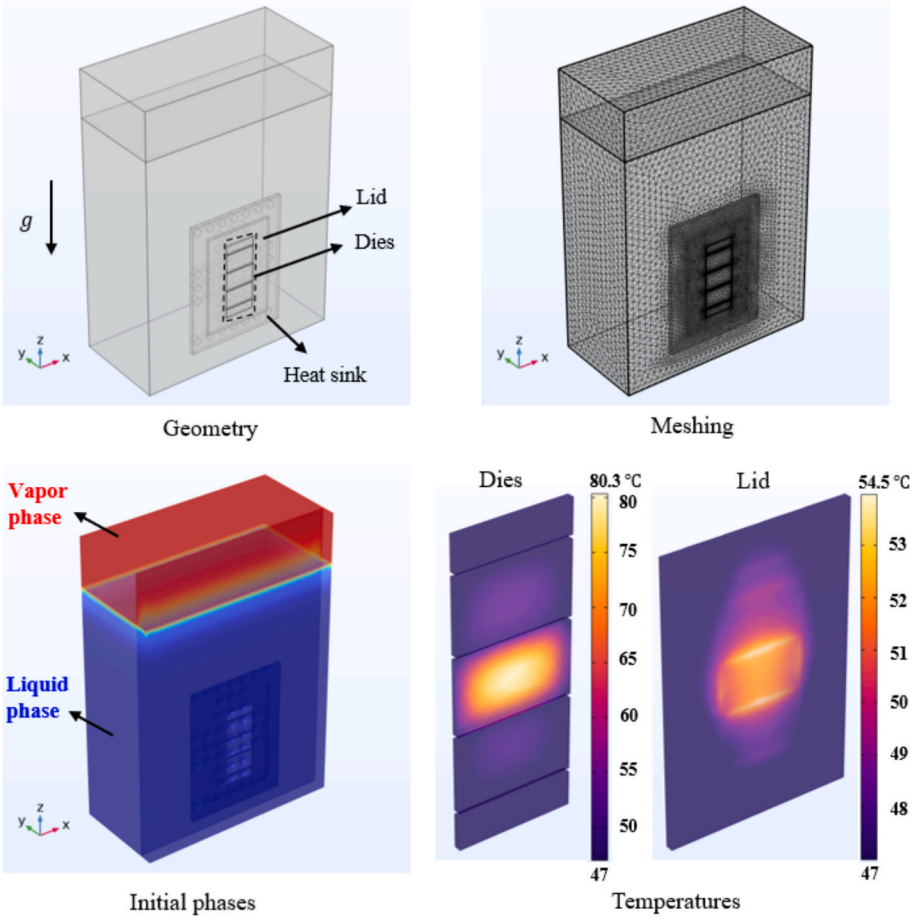

Fig. 7. Temperature distributions of dies and lid obtained via numerical simulation.

in Fig. 1), attributed to simplifications such as the use of thicker unpackage-style dies for computational efficiency. The simulated thermal gradient shows a maximum difference of 7.7 °C of lid, which is similar with experimental measurements. This result underscores the need for more effective thermal uniformity strategies in future two-phase cooling designs.

Heat is conducted from the dies to the heat sink and subsequently dissipated to the coolant through boiling. The overall thermal resistance, R_{tot}, which governs both the total heat dissipation rate and the temperature at the base of the dies, is defined as [44]:

$$R_{tot} = R_{Die} + R_{TIM} + R_{sp} + R_f + R_b = \sum R_i = \frac{\Delta \overline{T}_i}{Q} \quad (6)$$

where $\Delta \overline{T}_{ii}$ represents the temperature drop across each material layer (die, thermal interface material, heat sink base, and fins) and Q is the total power input. To investigate the impact of small die size and non-uniform power distribution on thermal spreading resistance and peak temperature, the simulation model was adapted by replacing multiple dies with a single die heat source, while maintaining the total power at 300 W and all other boundary conditions unchanged (see supplemental Fig. 1). The total thermal resistance was calculated as $R_{tot} = (T_{max} - T_{sat})/Q$. Results show that R_{tot} decreased from 0.111 °C/W in the multi-die configuration to 0.062 °C/W in the single-die case – a reduction of 0.049 °C/W. Correspondingly, the maximum die temperature dropped by 14.7 °C. These findings confirm that the combination of small heat source dimensions and uneven power distribution intensifies lateral thermal spreading resistance, leading to elevated peak temperatures. The simulation results are associated with the bubble aggregation behavior in the central area of the heat sink, as observed in Fig. 6 (f), and the temperature curve measured in Fig. 5 (a). A related simulation study [44] suggested that optimizing the heat source-to-sink area ratio and employing high-thermal-conductivity materials can help mitigate spreading resistance. However, in the present system, where the TTV package size is fixed – a conventional copper heat sink alone proves inadequate in overcoming the high thermal spreading resistance. Simulation-based analysis indicates that the integration of higher-conductivity materials can contribute to reducing this resistance.

4.3. Heat spreading optimization and performance of integrated architecture

Given the challenge of localized temperature rise due to thermal spreading resistance and uneven heat distribution, the vapor chamber (VC) emerges as a preferred heat spreader owing to its exceptionally high thermal conductivity. Commercial VCs typically exhibit an effective thermal conductivity of 2000–5000 W/(m • K), substantially exceeding that of pure copper. Although prior research [32] has identified the potential of VCs as heat spreaders in HFE-7100 coolant for high-heat-flux server cooling, comparative studies evaluating performance before and after VC integration have been lacking. To address this gap, we developed a hybrid cooling architecture that combines a vapor chamber as a heat spreader with an enhanced heat sink (denoted as EHS-VC), aimed at mitigating temperature non-uniformity and reduce the peak temperature. The optimized assembly incorporates a thinned 2 mm EHS base – reduced from the original 4 mm – bonded to a commercially sourced VC. As illustrated in Fig. 8 (a), the VC features external dimensions of 136 mm × 96 mm × 3.5 mm. An aluminum alloy frame provides structural support, while a nickel-plated surface ensures oxidation resistance.

Experimental results (Fig. 9 (a)–(d)) confirm a breakthrough in thermal performance: at 600 W, the maximum hotspot temperature (T_1) drops to 64.3 °C, the mean temperature decreases by 22.1 % to 62.6 °C, and the average thermal resistance is reduced by 6.4 % to 0.026 °C/W. Most notably, the maximum temperature difference (ΔT_{max}) plummeted 75.1 % to 3.8 °C, underscoring the efficacy of phase-change-mediated heat spreading within the VC (Fig. 9 (d)). This high-thermal-conductivity spreading mechanism directly alleviates the thermal gradient issues identified earlier.

Table 2 summarizes thermal performance metrics from previously reported two-phase immersion cooling systems developed by chip manufacturers and server providers. These studies primarily focus on

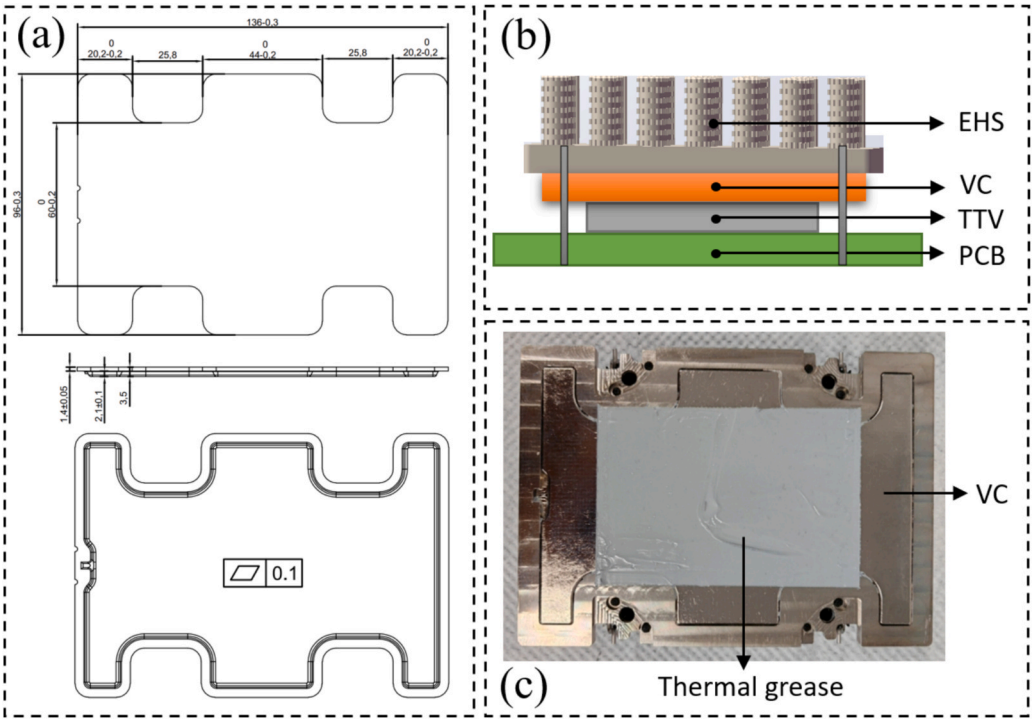

Fig. 8. The issue of substantial temperature difference and heat dissipation is tackled by integrating the vapor chamber. (a) Design drawing of the vapor chamber according to the EHS base size, (b) schematic diagram of integrating the vapor chamber with EHS, (c) bottom view of integrated the vapor chamber with EHS.

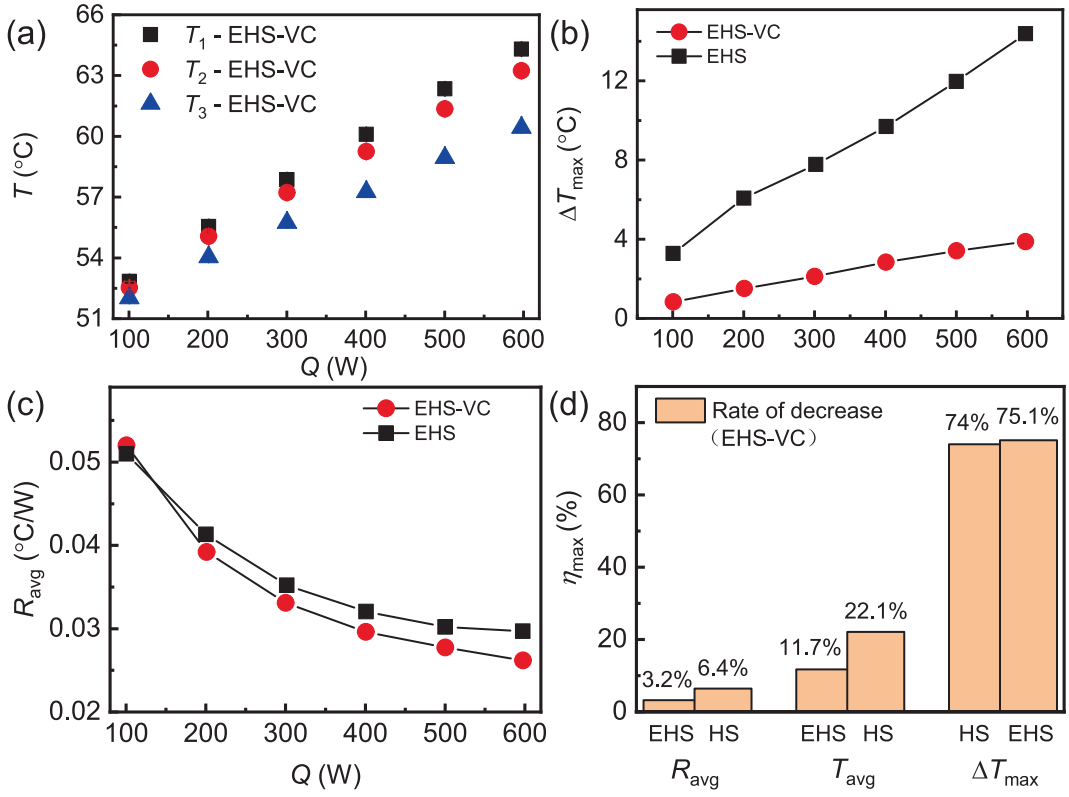

Fig. 9. The issue of substantial temperature difference and heat dissipation is tackled by integrating the vapor chamber. (a) Temperature distribution corresponding to each thermocouple element after integration of VC, (b) maximum temperature difference of EHS-VC comparing with EHS, (c) average resistance of EHS-VC with VC comparing with EHS, (d) comparison of the proportion of the enhancement in heat dissipation performance.

Table 2
Experimental studies results in selected literatures.

Surface	Coolant	Power (W)	Heat source	T_{max}(°C)	Thermal resistance (°C/W)
Removable boiling layer [27]	FC-72	600	TTV	74	~0.03
10 mm-pin-fins 3D printing [28]	FC-72	600	TTV	~74.5	~0.03
10 mm-pin-fins MIM [28]	FC-72	600	TTV	~71	~0.025
Boiler with VC [13]	HT55	350 900	BGA TTV CoWoS TTV	~81.4 92.2	~0.061 0.0355
Steel [30]	YL-10	600	Film heater	69.94	~ 0.0374
This study	Noah – 2100A	600	Intel TTV	64.3	0.026

minimizing peak chip temperature, motivated by the fact that CPU performance and reliability degrade by approximately 10 % for every 2 °C increase beyond 70 °C [45]. In most cases, the reported maximum case temperatures approach or exceed 70 °C [30]. Moreover, many studies rely on single-point thermocouple measurements, thereby overlooking lateral temperature variation. While advanced packaging solutions such as CoWoS [13] account for thermal non-uniformity and enable total power dissipation up to 900 W, the resulting maximum temperature and thermal resistance remain relatively high, even with a vapor chamber base. Although a minimum thermal resistance of 0.025 °C/W has been achieved using more complex lidded packaging processes [28], the EHS-VC architecture presented here offers a competitive balance of performance and manufacturability. Furthermore, the experimental results of the EHS-VC from this study were compared with the boiling curve data reported in figure 14 of Ref. [30], as illustrated in Fig. 10. The boiling curves exhibit similar trends, which can be attributed to the comparable thermophysical properties of the coolants used in the studies. For instance, YL-10 experiment employed a simple steel plate as the cooling surface (see Table 2), whereas the present study utilizes a VC with a larger surface area for convection. These design improvements contribute to enhanced boiling performance in our experiments, thereby confirming both the reliability of the current results and the robustness of the experimental setup. In summary, while earlier

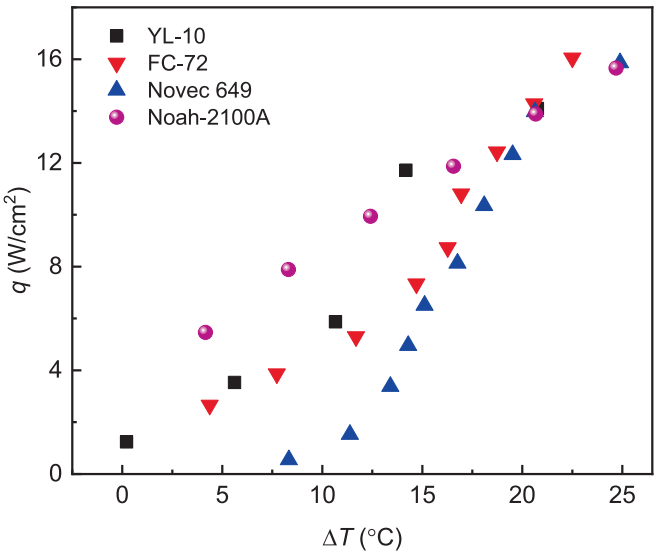

Fig. 10. Comparison between the boiling curves in this work and studies in Ref. [30].

studies mainly focused on augmenting nucleation sites or increasing surface area on heat sink structures, our EHS adopts a multi-scale approach and integrates the EHS with a VC, which further overcome thermal spreading resistance, a challenge seldom tackled in earlier immersion cooling studies.

Following the ongoing trend of device scaling under Moore's Law [46], power dissipation of high-performance CPUs and GPUs is projected to exceed 1,000 W [28]. To assess the cooling capability of our system under such conditions, a second-order polynomial regression was applied to the experimental thermal data ($T_{mean} = aQ^2 + bQ + c$, with coefficients a = 7×10^6 b = 0.25, and c = 49.9). As summarized in Table 3 and illustrated in Fig. 11, the proposed model predicts a mean case temperature of 68.2 °C under kilowatt-level power, assuming equivalent boundary conditions. It should be emphasized, however, that this extrapolation is derived from data obtained within the 0–600 W range and lacks experimental validation at higher loads. The regression does not incorporate potential nonlinear effects such as phase-change instability or thermal spreading resistance at extreme heat fluxes. Additional factors, including altered bubble dynamics, local dry-out risk, or condenser limitations under intense vapor generation, could significantly degrade practical performance. Thus, while the model provides a useful preliminary estimate, actual performance under kilowatt-class operation must be verified experimentally. Existing literature [28] suggests that structural enhancements, such as increasing the finned area (e.g., extending the fin height H_c to 10 mm) or optimizing the geometry, could help maintain case temperatures below 65 °C even at kilowatt levels. Such design refinements represent a promising pathway for adapting the proposed cooling strategy to next-generation high-power chips. It should be noted, however, that the current design is tailored to standard server packages; adaptation to emerging chiplet – based architectures would require further geometric re-optimization. In addition, the present approach still faces certain limitations, including reliance on high–thermal-conductivity materials that increase cost, as well as a multi-scale fabrication process that demands precise manufacturing control.

Table 3
Prediction of the temperature under higher power loading up to 1 kW.

Power supply (W)	Mean temperature (°C)
700	64.2
800	65.7
900	67.1
1000	68.2

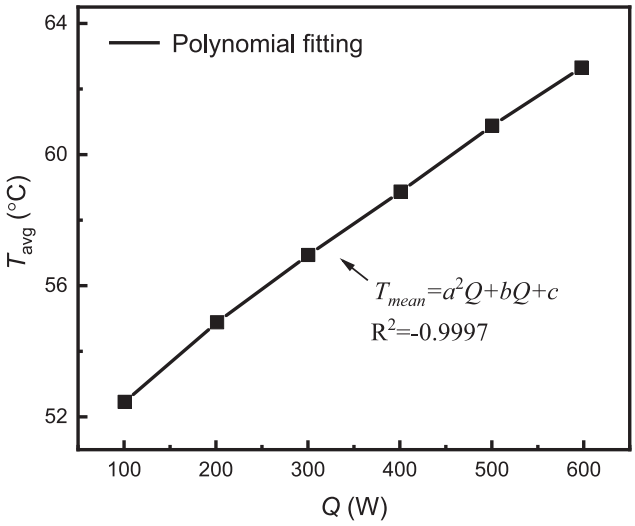

Fig. 11. Data fitting for the mean temperature of EHS-VC.

5. Conclusions and outlook

Two-phase immersion cooling (TPIC) presents significant potential for enhancing CPU performance and system-level energy efficiency. This study developed a monolithic high-performance heat sink to replace conventional air-cooled solutions in TPIC systems. The proposed architecture synergistically integrates macro pin-fins (featuring micro-serrations and nano-coatings) with a vapor chamber that acts as both a heat spreader and a structural base. This integrated design effectively reduces the peak chip temperature while mitigating lateral thermal heterogeneity. Experimental results demonstrate that the hybrid design maintains a maximum case temperature below 65 °C at 600 W heat load, with a total thermal resistance under 0.026 °C/W. Compared to a pure copper heat sink, which exhibited a spatial temperature gradient of 14.3 °C, the vapor chamber-assisted configuration improved temperature uniformity by reducing the maximum temperature difference by 75 % (to 3.8 °C). It also lowered the average thermal resistance by 6.4 % and the mean temperature by 22.1 % – a combination of benefits not systematically reported in prior VC-based immersion cooling studies. Data extrapolation suggests this approach is scalable for kilowatt-level cooling demands.

Despite these advances, the widespread adoption of immersion cooling is still constrained by high material costs and unresolved compatibility issues between coolants and electronic components. Future work should prioritize the development of bio-derived or recyclable coolant alternatives to enhance environmental sustainability. A comparative study of nucleation enhancement techniques, such as the graphene coating applied in this work versus sintered porous copper or carbon nanotube arrays would help to quantitatively assess their efficiency and cost-effectiveness. Furthermore, systematic optimization of the coupling between macro-fin spacing and nanostructure density through parametric studies could help overcome the trade-off between thermal resistance and temperature uniformity identified in this study. Finally, thermal cycle tests and aging analysis of materials and modules under long-term operating conditions represent critical directions for future research.

CRediT authorship contribution statement

Bin Li: Writing – original draft, Investigation, Data curation. **Long Pan:** Validation, Formal analysis. **Anqi Liu:** Methodology, Formal analysis. **Jingyang Hao:** Visualization, Supervision, Resources. **Bingyang Cao:** Visualization, Supervision, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.tsep.2026.104495.

Data availability

Data will be made available on request.

References

[1] Y. Zhang, K. Shan, X. Li, H. Li, S. Wang, Research and Technologies for next-generation high-temperature data centers – State-of-the-arts and future perspectives, Renew. Sust. Energ. Rev. 171 (2023) 112991.
[2] Z.-Q. Yu, M.-T. Li, B.-Y. Cao, A comprehensive review on microchannel heat sinks for electronics cooling, Int. J. Extreme Manuf. 6 (2) (2024) 022005.
[3] S. Zheng, C. Su, X. Yang, Y. Zhang, K. Duan, Y. Zhang, Z. Huang, Y. Zhang, F. Liu, J. Wei, A comprehensive review of single-phase immersion cooling in data centres, Appl. Therm. Eng. 272 (2025) 126385.
[4] S. Liu, Z. Xu, Z. Wang, X. Li, H. Sun, X. Zhang, H. Zhang, Optimization and comprehensive evaluation of liquid cooling tank for single-phase immersion cooling data center, Appl. Therm. Eng. 245 (2024) 122864.
[5] D. Ni, F. Yu, CFD simulation study of flow equalisation plate model in single-phase immersion liquid cooling for servers, Therm. Sci. Eng. Prog. 47 (2024) 102268.
[6] H. Alissa, T. Nick, A. Raniwala, A. Arribas Herranz, K. Frost, I. Manousakis, K. Lio, B. Warrier, V. Oruganti, T.J. DiCaprio, K. Oseen-Senda, B. Ramakrishnan, N. Gupta, R. Bianchini, J. Kleewein, C. Belady, M. Fontoura, J. Sinistore, M. Natarajan, L. Johnson, V. Mealing, P. Arshi, M. Frieze, Using life cycle assessment to drive innovation for sustainable cool clouds, Nature 641 (8062) (2025) 331–338.
[7] X. Yuan, X. Zhou, Y. Pan, R. Kosonen, H. Cai, Y. Gao, Y. Wang, Phase change cooling in data centers: a review, Energ. Buildings 236 (2021) 110764.
[8] Z. Li, H. Luo, Y. Jiang, H. Liu, L. Xu, K. Cao, H. Wu, P. Gao, H. Liu, Comprehensive review and future prospects on chip-scale thermal management: core of data center's thermal management, Appl. Therm. Eng. 251 (2024) 123612.
[9] C. Zhang, H. Wang, Y. Huang, L. Zhang, Y. Chen, Immersion liquid cooling for electronics: Materials, systems, applications and prospects, Renew. Sust. Energ. Rev. 208 (2025) 114989.
[10] B.B. Kanbur, C. Wu, S. Fan, W. Tong, F. Duan, Two-phase liquid-immersion data center cooling system: experimental performance and thermoeconomic analysis, Int. J. Refrig. 118 (2020) 290–301.
[11] J.M. Shah, T. Crandall, P.E. Tuma, Chip level thermal performance measurements in two-phase immersion cooling, J. Electron. Packaging 145 (4) (2023).
[12] K.-H. Chu, R. Enright, E.N. Wang, Structured surfaces for enhanced pool boiling heat transfer, Appl. Phys. Lett. 100 (24) (2012) 241603.
[13] P.Y. Lin, S.L. Kuo, K. Yan, W.M. Chen, M.D.D. Liao, Advanced thermal integration for HPC packages with two-phase immersion cooling, in: 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), 2022, pp. 566–573.
[14] G. Song, X. Ma, P. Xu, Y. Feng, Y. Zhang, J. Wei, Experimental study of pool boiling heat transfer on hybrid surface coupled micro-pin-finned, Int. J. Heat Fluid Fl. 108 (2024) 109467.
[15] Y. Ma, Y. Bao, J. Li, Heat transfer dependence of power usage effectiveness of an augmented two-phase immersion cooling system for high-power servers, Energy 323 (2025) 135853.
[16] L.L. Manetti, A.S.O.H. Moita, R.R. de Souza, E.M. Cardoso, Effect of copper foam thickness on pool boiling heat transfer of HFE-7100, Int. J. Heat Mass Tran. 152 (2020) 119547.
[17] L. Liu, C. Fu, S. Li, L. Zhu, F. Ma, Z. Zeng, G. Wang, Superspreading surface with hierarchical porous structure for highly efficient vapor–liquid phase change heat dissipation, Small 20 (44) (2024) 2403040.
[18] J. Li, Y. Zhao, J. Ma, W. Fu, X. Yan, K.F. Rabbi, N. Miljkovic, Superior antidegeneration hierarchical nanoengineered wicking surfaces for boiling enhancement, Adv. Funct. Mater. 32 (8) (2022) 2108836.
[19] C. Huang, H. Wang, E. Lichtfouse, Y. Tang, H. Xiang, Experimental study of multilayer gradient copper foam effect on pool boiling heat transfer performance and gas-liquid behavior characteristics, Int. J. Therm. Sci. 183 (2023) 107856.
[20] C.K. Yu, D.C. Lu, Pool boiling heat transfer on horizontal rectangular fin array in saturated FC-72, Int. J. Heat Mass Tran. 50 (17) (2007) 3624–3637.
[21] Y. Yang, X. Ji, J. Xu, Pool boiling heat transfer on copper foam covers with water as working fluid, Int. J. Therm. Sci. 49 (7) (2010) 1227–1237.
[22] S. Jun, H. Wi, A. Gurung, M. Amaya, S.M. You, Pool Boiling Heat transfer Enhancement of Water using Brazed Copper Microporous Coatings, J. Heat Trans. 138 (7) (2016).
[23] W. Zhou, H. Ma, Y. Hu, G. Xia, Nucleate boiling enhancement of FC-72 on the carbon nanotube buckypaper for two-phase immersion cooling, Int. J. Heat Mass Tran. 228 (2024) 125639.
[24] Y. Sun, Y. Tang, S. Zhang, W. Yuan, H. Tang, A review on fabrication and pool boiling enhancement of three-dimensional complex structures, Renew. Sust. Energ. Rev. 162 (2022) 112437.
[25] Q. Cao, X. Sun, Q. Li, B. Liu, L. Chang, Enhanced pool boiling heat transfer by coupling multiscale structures and mixed wettability, Int. J. Therm. Sci. 208 (2025) 109396.
[26] S.G. Kandlikar, Enhanced Macroconvection Mechanism with Separate Liquid–Vapor Pathways to Improve Pool Boiling Performance, J. Heat Trans. 139 (5) (2017).
[27] J. Chuang, J. Yang, D. Shia, Y.L. Li, A Low Profile Two-phase Immersion Cooling Stack-up based on Detachable Boiling Enhancement Layer on Lidded Electronic packages, in: 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), 2022, pp. 1567–1572.
[28] J. Chuang, J. Yang, D. Shia, Y.L. Li, in: Lidded Electronic Package with Boiling Enhancement Features, in, 2021, pp. 1596–1601.
[29] G. Pottker, A. Van Wassen, D.R. Brandt, A New Low-GWP Dielectric Fluid for Two-Phase Immersion Cooling, in, 2023.
[30] X. Wu, J. Yang, Y. Liu, Y. Zhuang, S. Luo, Y. Yan, L. Xiao, X. Han, Investigations on heat dissipation performance and overall characteristics of two-phase liquid immersion cooling systems for data center, Int. J. Heat Mass Tran. 239 (2025) 126575.
[31] X. Sun, Z. Han, X. Li, Simulation study on cooling effect of two-phase liquid-immersion cabinet in data center, Appl. Therm. Eng. 207 (2022) 118142.
[32] G. Zhou, J. Zhou, X. Huai, F. Zhou, Y. Jiang, A two-phase liquid immersion cooling strategy utilizing vapor chamber heat spreader for data center servers, Appl. Therm. Eng. 210 (2022) 118289.
[33] L. Zhejiang Noah Fluorochemical Co., Noah® 2100A Two-phase electronic coolant, product Properties, May 22, 2025.
[34] M. Yang, M.-T. Li, Y.-C. Hua, W. Wang, B.-Y. Cao, Experimental study on single-phase hybrid microchannel cooling using HFE-7100 for liquid-cooled chips, Int. J. Heat Mass Tran. 160 (2020) 120230.
[35] X. Li, L. Lv, X. Wang, J. Li, Transient thermodynamic response and boiling heat transfer limit of dielectric liquids in a two-phase closed direct immersion cooling system, Therm. Sci. Eng. Prog. 25 (2021) 100986.
[36] J. Chuang, J. Yang, D. Shia, Y.L. Li, Boiling Enhanced Lidded Server packages for Two-phase Immersion Cooling using Three-Dimensional Metal Printing and Metal Injection Molding Technologies, J. Electron. Packaging 143 (4) (2021).
[37] Z. Xu, P. Zhang, C. Yu, W. Miao, Q. Chang, M. Qiu, Y. Li, Y. Tian, L. Jiang, Liquid-superspreading-boosted high-performance jet-flow boiling for enhancement of phase-change cooling, Adv. Mater. 35 (26) (2023) 2210557.
[38] B. Li, S. Lin, Y. Wang, Q. Yuan, S.W. Joo, L. Chen, Promoting rebound of impinging viscoelastic droplets on heated superhydrophobic surfaces, New J. Phys. 22 (12) (2020) 123001.
[39] C.C. Hsu, T.-L. Chang, Y.-C. Chang, C.-P. Wang, Enhancing boiling heat transfer by ultrafast laser texturing of groove structures on thin-film graphene surfaces, Therm. Sci. Eng. Prog. 61 (2025) 103510.
[40] B. Li, A.A. Mehrizi, S. Lin, S. Joo, L. Chen, Dynamic behaviors of impinging viscoelastic droplets on superhydrophobic surfaces heated above the boiling temperature, Int. J. Heat Mass Tran. 183 (2022) 122080.
[41] F. Ejaz, B. Kwon, Two-phase active immersion cooling for vertically mounted electronics with interchip component-assisted bubble departure, Int. Commun. Heat Mass 159 (2024) 107981.
[42] M. Zhao, W. Gong, W. Gong, Y. Li, S. Xu, Two-phase immersion cooling of simulated server chips using HFE-7100, in: 2024 5th International Conference on Computer Engineering and Application (ICCEA), 2024, pp. 323–328.
[43] Z. Wang, X. Zheng, C. Chryssostomidis, G.E. Karniadakis, A phase-field method for boiling heat transfer, J. Comput. Phys. 435 (2021) 110239.
[44] A. Ali, Thermal performance and stress analysis of heat spreaders for immersion cooling applications, Appl. Therm. Eng. 181 (2020) 115984.
[45] A.M. Haywood, J. Sherbeck, P. Phelan, G. Varsamopoulos, S.K.S. Gupta, The relationship among CPU utilization, temperature, and thermal power for waste heat utilization, Energ. Convers, Manage 95 (2015) 297–303.
[46] S. Du, Q. Zhang, S. Zou, F. Meng, L. Liu, Simulation analysis on energy consumption and economy of CPU cooling system based on loop heat pipe for data center, Therm. Sci. Eng. Prog. 45 (2023) 102115.